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A Comparative Study of Approximate Adders and Multipliers

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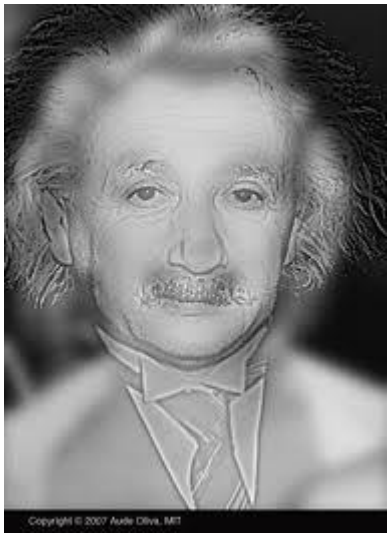
Outline

- **Motivation and Introduction**
- **Review and Classification of Approximate Adders**
- **Comparison of the Approximate Adders**
  - Error Characteristics
  - Circuit Characteristics
- **Review and Classification of Approximate Multipliers**
- **Comparison of the Approximate Multipliers**
  - Error Characteristics
  - Circuit Characteristics
- **Conclusion**

Motivation

- The physical dimensions of CMOS devices have been scaling and approaching a few nanometers.
  - Improving circuit performance of digital circuits becomes increasingly difficult.
  - Energy-efficiency is of paramount concern in digital system design.
- Computing becomes increasingly heavy with multimedia processing (audio, video, graphics, and image), recognition, search, machine learning and data mining.



- A common characteristic: a perfect result is not necessary and an approximate or less-than-optimal result is sufficient
  - Human perception is not sensitive to high frequency changes.
  - Natural noise floor due to quantization noise.

Error-Resilient Paradigms

- How can we exploit a system's ability for imprecision-tolerance and energy reduction?

- **Approximate Computing**
  - Does not involve assumptions on the stochastic nature of any underlying processes implementing the system. Utilizes statistical properties of data and algorithms to trade quality for energy reduction.

- **Stochastic Computing**
  - Real numbers are represented by random binary bit streams that are usually implemented in series (or parallel) and in time (or space). Information is carried on the statistics of the binary streams.

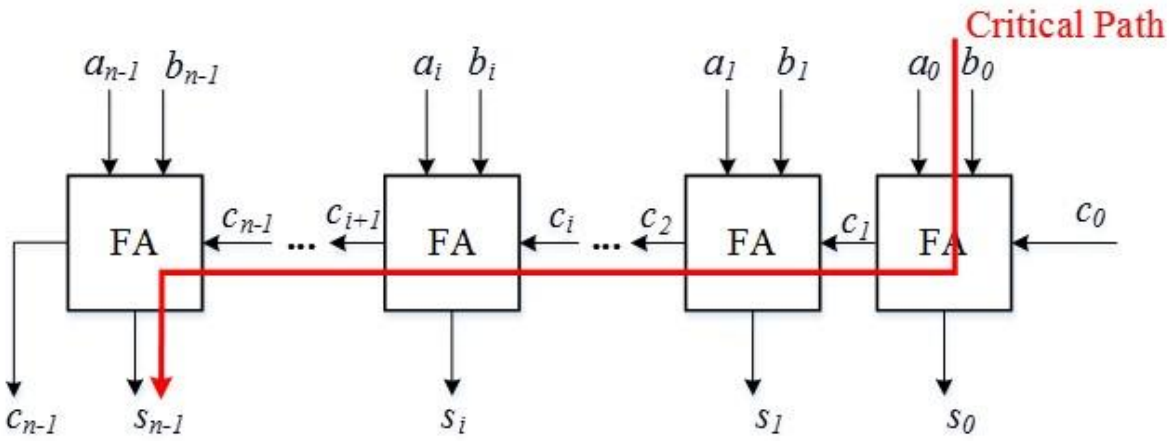
- **Probabilistic Computing**
  - Exploits intrinsic probabilistic behavior of the underlying circuit fabric, most explicitly, of the stochastic behavior of a binary switch under the influence of thermal noise.

J. Han and M. Orshansky. Approximate Computing: An Emerging Paradigm For Energy-Efficient Design. In ETS, pages 1-6, Avignon, France, 2013.

Approximately Designed Adders and Multipliers

- Effort in approximate computing covers a broad spectrum of research, ranging from those addressing issues at circuit and system levels, up to those at software and application levels,
- **We focus on approximate hardware design and, in particular, approximate arithmetic circuits of adders and multipliers, or approximately designed adders and multipliers.**

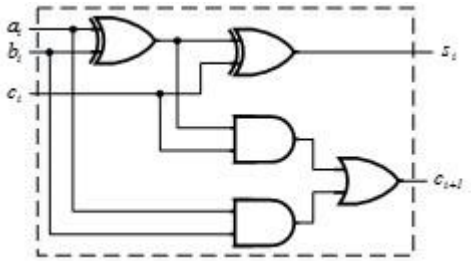
Ripple-Carry Adder (RCA)



The *n*-bit ripple-carry adder.

$$s_i = a_i \oplus b_i \oplus c_i$$

$$c_{i+1} = a_i b_i + a_i c_i + b_i c_i$$

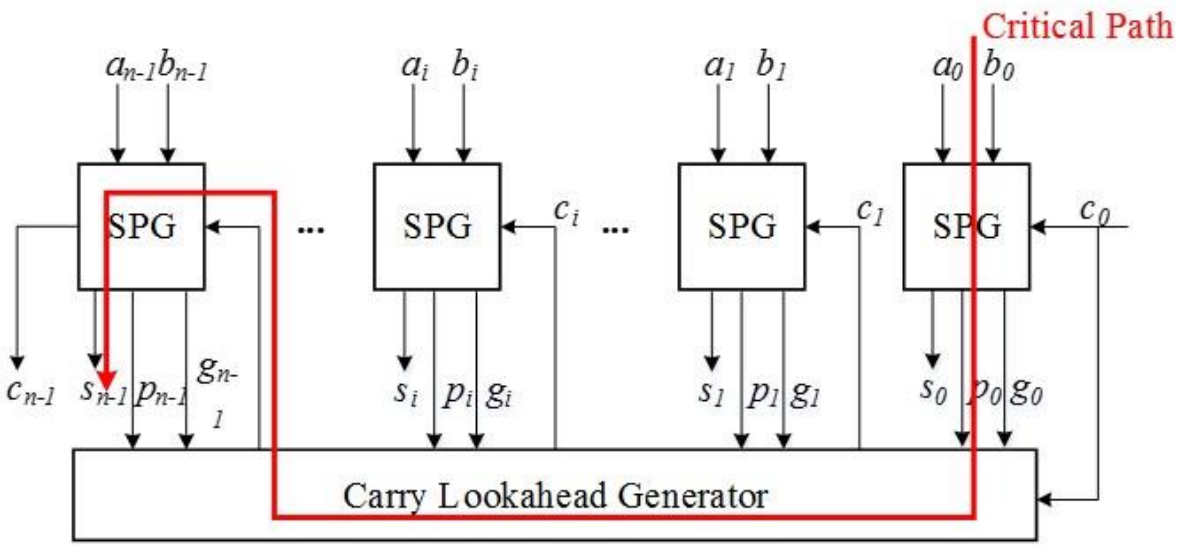


The schematic of a full adder (FA).

$$Critical\ path\colon O(n)$$

$$Circuit\ area\colon O(n)$$

Carry Lookahead Adder (CLA)

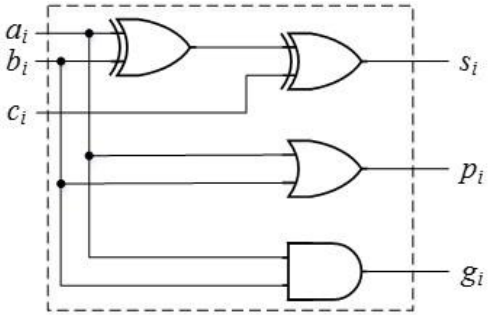


An *n*-bit carry lookahead adder.

$$s_i = a_i \oplus b_i \oplus c_i$$

$$g_i = a_i b_i$$

$$p_i = a_i + b_i$$



The schematic of the sum, propagate and generate signal generator (SPG).

$$Critical\ path\text{: } O(\log(n))$$

$$Circuit\ area\text{: } O(n\log(n))$$

Approximate Adders: A Classification

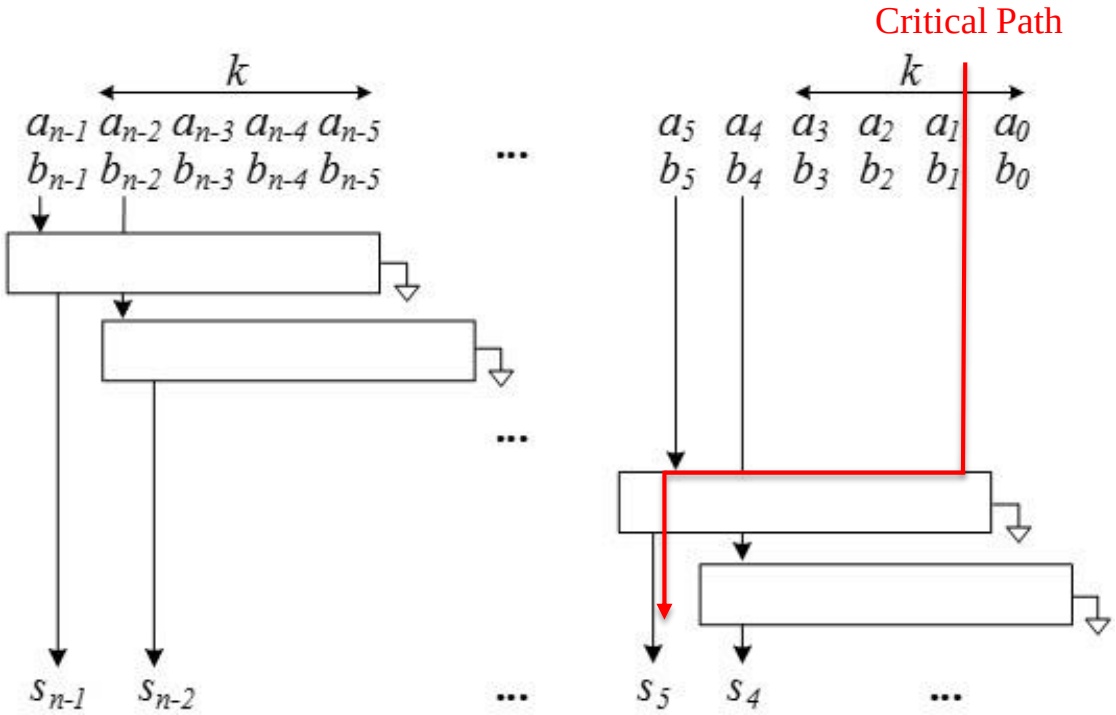
We classify the approximate adders into four categories:

- **Speculative Adders**
  - For a 128-bit adder, the probability that the carry propagation chain is longer than 12 and 18 are 1% and 0.01%, respectively.*
  - Therefore, k bits are used to speculate the carry for each sum bit ($k < n$).
- **Segmented Adders**
  - An n-bit adder is divided into a number of smaller k-bit sub-adders.
  - The carry may be generated by using different methods.
- **Carry-Select Adders**
  - Multiple sub-circuits are used to compute the sum for different carry values, and the result is selected by the carry of a sub-circuit.
- **Approximate Full Adders**

**A. K. Verma, P. Brisk, and P. Ienne. Variable latency speculative addition: A new paradigm for arithmetic circuit design. In DATE, pages 1250 - 1255, 2008.*

Speculative Adders

The almost correct adder (ACA):



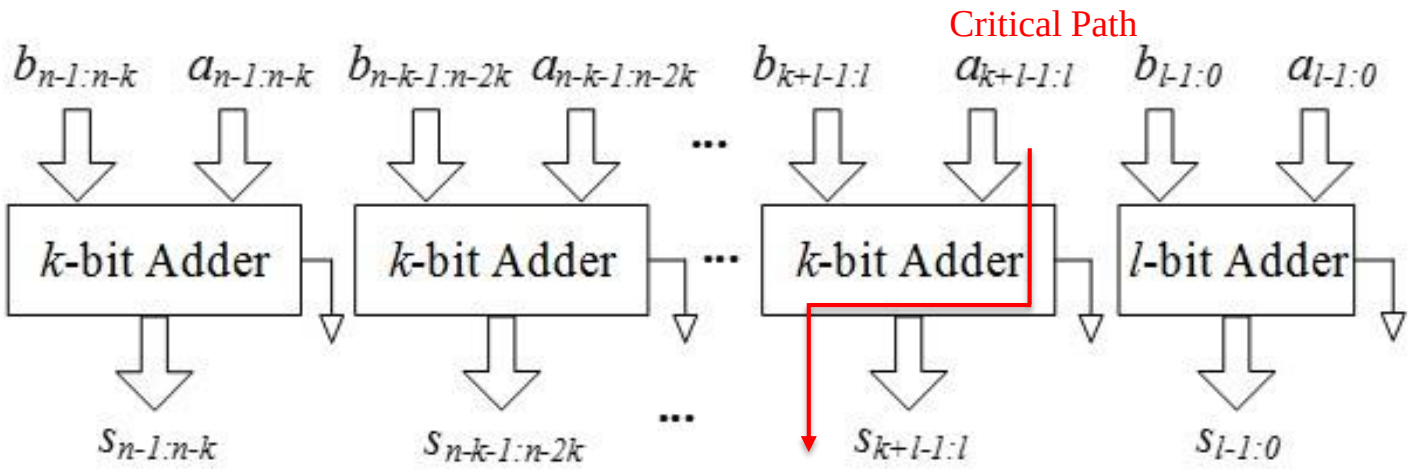
The *n*-bit almost correct adder (ACA).

$Critical\ path\colon\ O(\log(k))$ $\quad$ $Circuit\ area\colon\ O((n-k)k\log(k))$

A. K. Verma, P. Brisk, and P. Ienne. Variable latency speculative addition: A new paradigm for arithmetic circuit design. In DATE, pages 1250 - 1255, 2008.

Segmented Adders (1)

The equal segmentation adder (ESA):



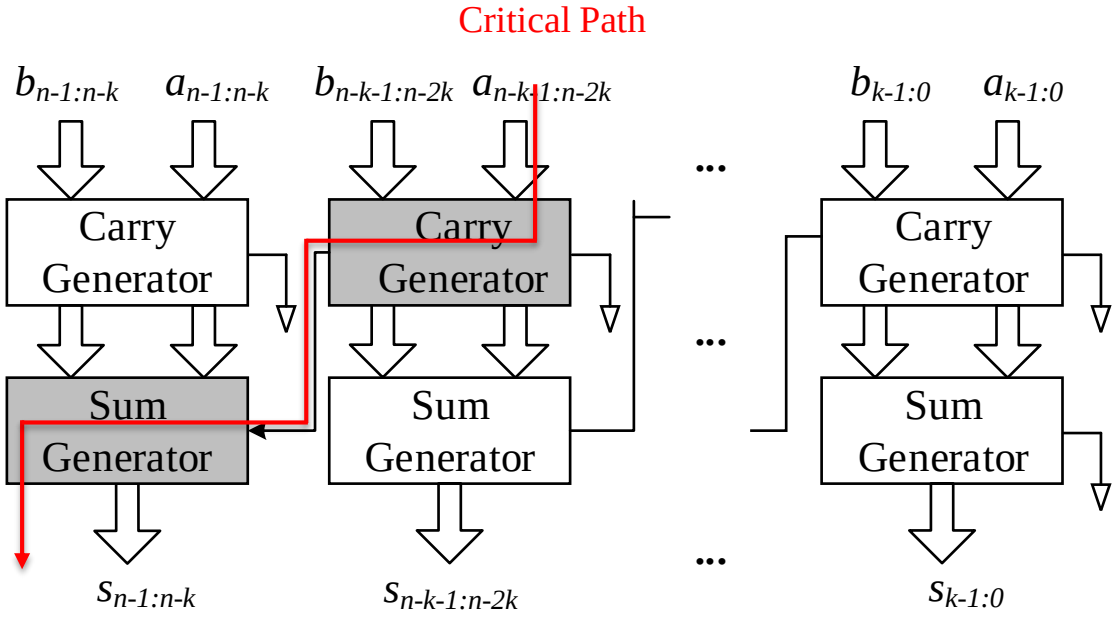
The n-bit equal segmentation adder (ESA) ($l \leq k$).

$Critical\ path\colon O(\log(k))$ $Circuit\ area\colon O(n\log(k))$

D. Mohapatra, V. Chippa, A. Raghunathan, and K. Roy. Design of voltage-scalable meta-functions for approximate computing. In DATE, pages 1-6, 2011.

Segmented Adders (2)

The error-tolerant adder type II (ETAII):



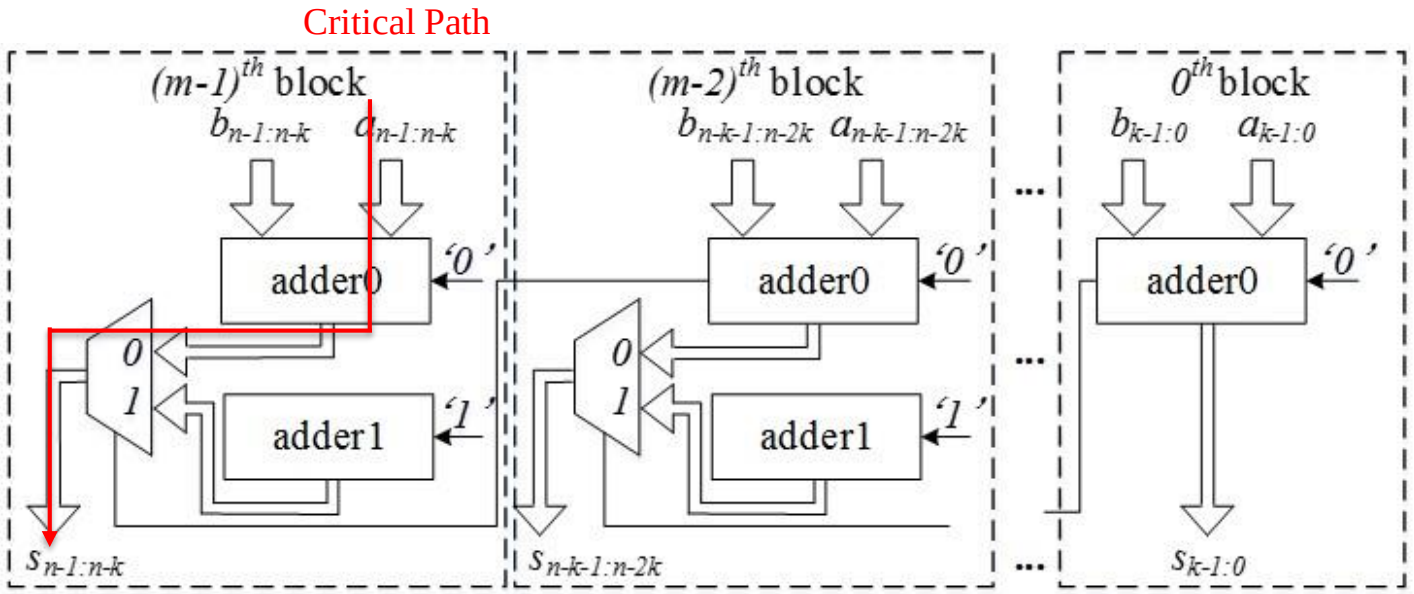
The *n*-bit error-tolerant adder type II (ETAII).

$Critical\ path\colon O(\log(k))$ $Circuit\ area\colon O(n\log(k))$

N. Zhu, W. L. Goh, and K. S. Yeo. An enhanced low-power high-speed adder for error-tolerant application. In ISIC 2009, pages 69-72, 2009.

Carry Select Adders

The speculative carry selection adder (SCSA):



The *n*-bit speculative carry selection adder (SCSA).

$Critical\ path$: $t_{adder} + t_{mux}$

t_{adder}: $O(\log(k))$

t_{mux}: $delay\ of\ the\ multiplexer$

$Circuit\ area$: $A_{adder} + A_{mux}$

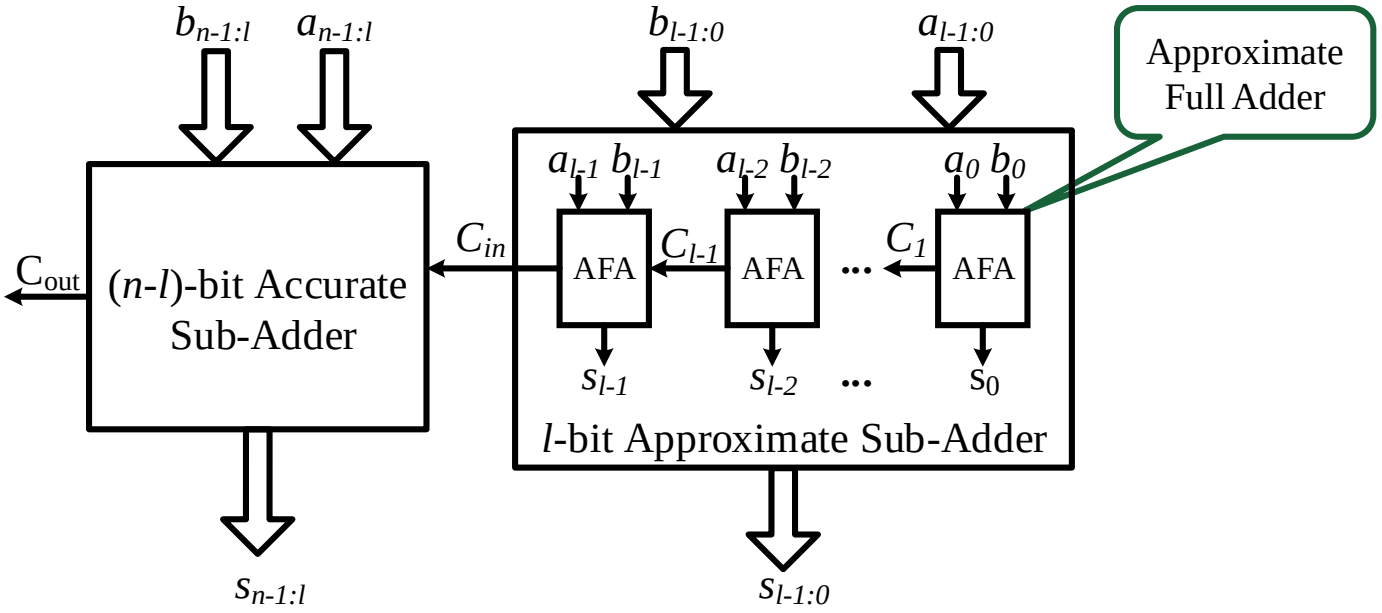
A_{adder}: $O(n\log(k))$

A_{mux}: $circuit\ area\ of\ the\ multiplexer$

K. Du, P. Varman, and K. Mohanram. High performance reliable variable latency carry select addition. In DATE, pages 1257-1262, 2012.

Approximate Full Adders

A general schematic:



The n-bit approximate adder using approximate full adders

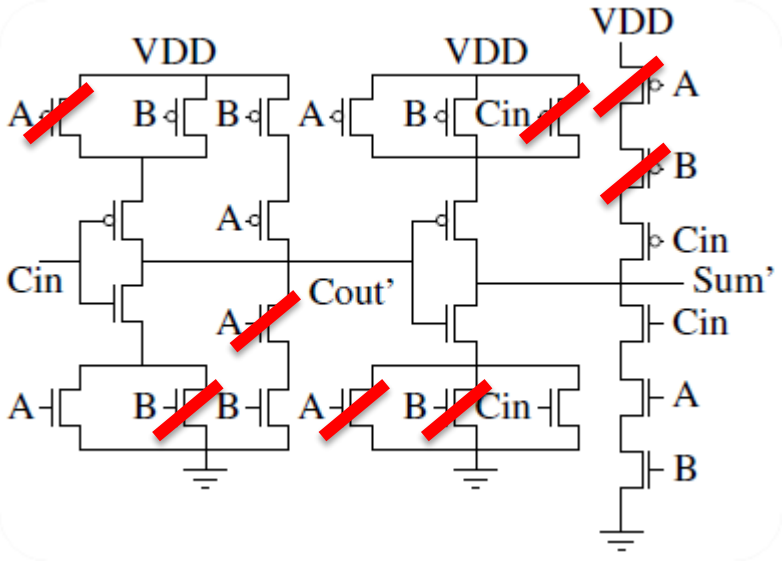
$Critical\ path$:

$t_{approximate\_adder} + t_{accurate\_adder}$

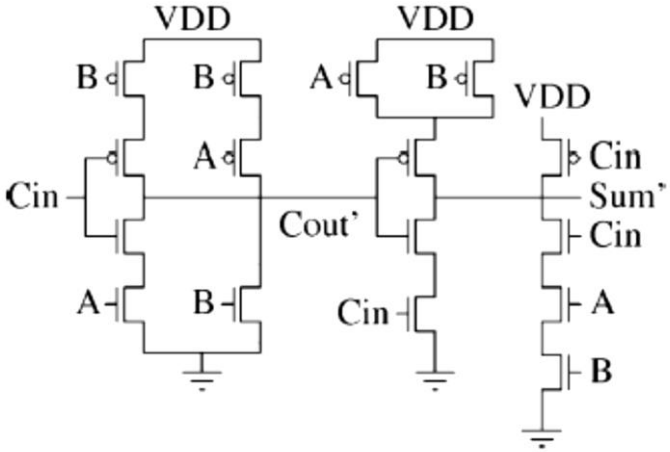
$Circuit\ area$:

$A_{approximate\_adder} + A_{accurate\_adder}$

Approximate Mirror Adders (AMAs)



The conventional mirror adder (MA).



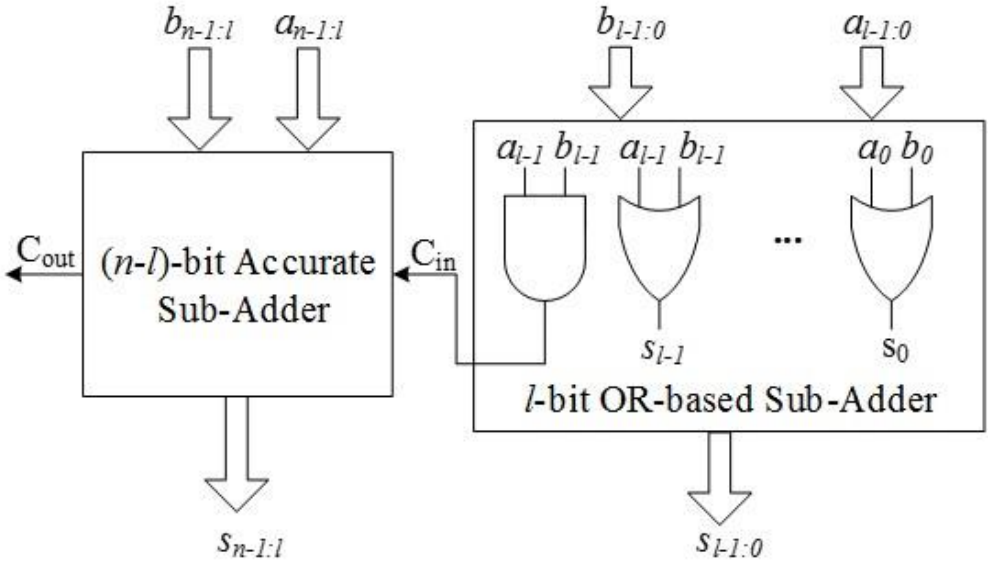
The mirror adder approximation 1 (AMA1).

The truth table for AMA1.

A	B	C_{in}	Sum'	C_{out1}
0	0	0	0	0
0	0	1	1	0
0	1	0	**0**	**1**
0	1	1	0	1
1	0	0	**0**	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

V. Gupta, D. Mohapatra, A. Raghunathan, and K. Roy. Low-power digital signal processing using approximate adders. IEEE Trans. CAD, 32(1):124-137, 2013.

Lower-part OR Adders (LOAs)



The n-bit lower-part-OR adder (LOA).

$Critical\ path$:
$O(\log(n-l))$

$Circuit\ area$:
$A_{adder} + (l \times A_{OR})$

A_{adder}: $O((n-l)log(n-l))$

A_{OR} : $circuit\ area\ of\ the\ OR\ gate.$

H. R. Mahdiani, A. Ahmadi, S. M. Fakhraie, and C. Lucas. Bio-Inspired Imprecise computational Blocks for Efficient VLSI Implementation of Soft-Computing Applications. IEEE Trans. Circuits Syst., 57(4):850-862, 2010.

A Brief Summary

Analysis of delay and circuit complexity of approximate adders.

Adder Type		Adder Name	Delay	Circuit Area
Conventional Adders		RCA	$O(n)$	$O(n)$
		CLA	$O(log(n))$	$O(nlog(n))$
Approxim-ate Adders	Speculative Adders	ACA [3]	$O(\log(k))$	$O((n-k)k\log(k))$
	Segmented Adders	**ESA [6]**	$\boldsymbol{O(\log(k))}$	$\boldsymbol{O(n\log(k))}$
		ETAII [4]	$\boldsymbol{O(\log(k))}$	$\boldsymbol{O(n\log(k))}$
		ACAA [5]	$O(\log(k))$	$O((n-k)\log(k))$
	Carry Select Adders	SCSA [7]	$t_{adder}+t_{mux}$	$A_{adder}+A_{mux}$
		CSA [8]	$O(\log(k))$	$A_{adder}+A_{carry}$
		CSPA [10]	$t_{adder}+t_{mux}$	$A_{adder}+A_{mux}+A_{carry}$
		CCA [11]	$t_{adder}+t_{mux}$	$A_{adder}+A_{mux}$
		GCSA [12]	$O(\log(k))$	$O(n\log(k))$
	Approximate Full Adders	LOA [13]	$O(\log(n-l))$	$A_{loa}+(l\times A_{OR})$

t_{adder}: $O(\log(k))$ A_{adder}: $O(n\log(k))$ A_{loa}: $O((n-l)\log(n-l))$

A_{carry}: circuit are of the carry prediction circuit

- ESA has the smallest delay and circuit area.
- ETAII, ACAA and SCSA have the same accuracy; ETAII is the most efficient design among them.

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Error Metrics

- **Error rate (ER)** is the probability of producing an incorrect result.
- **Error distance (ED)** is the arithmetic distance between an approximate result and the accurate result.

  If M' and M are the approximate and accurate results, $ED = |M' - M|$.
- **Relative error distance (RED)** is used to evaluate the relative difference between an approximate result and the accurate result.

  For M' and M, $RED = \frac{ED}{M}$.

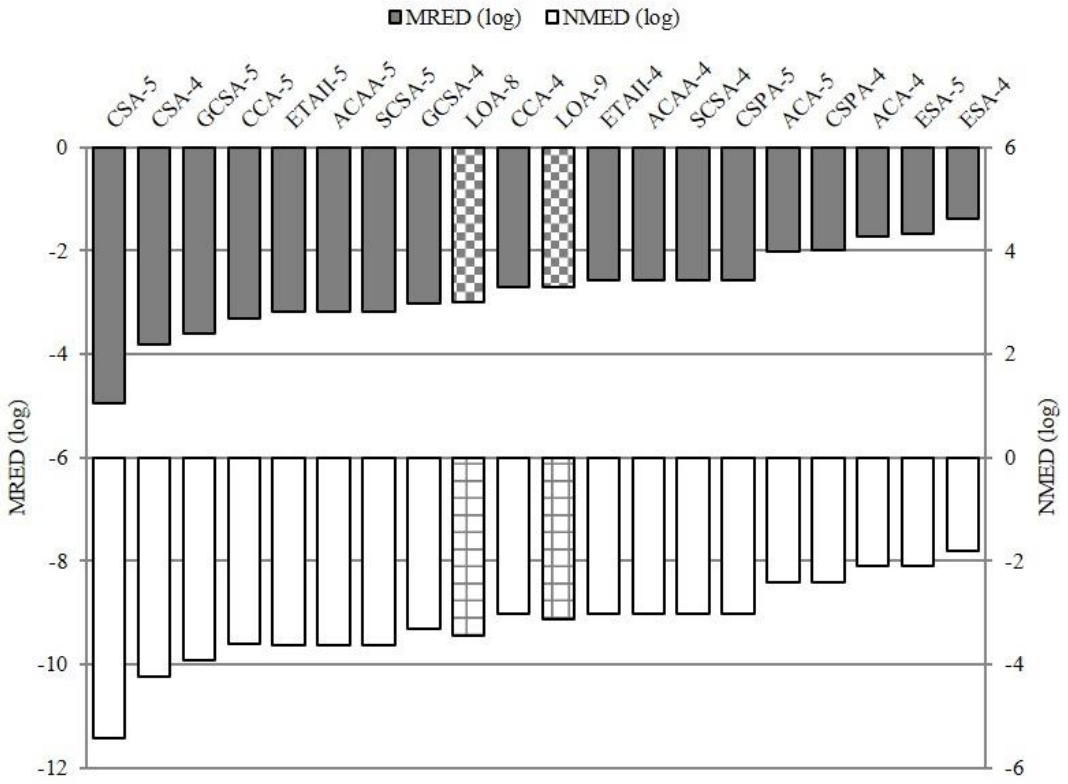
Error Metrics (cont'd)

- **Mean error distance (MED)** considers the average error distance for multiple inputs.
  - The MED increases exponentially with the number of approximate bits in an adder.
- **Normalized mean error distance (NMED)** is the normalization of MED by the maximum output value.
  - The NMED is a nearly invariant metric independent of the size of an adder
- **Mean relative error distance (MRED)** assesses the average relative error distance for multiple inputs.

J. Liang, J. Han, and F. Lombardi. New metrics for the reliability of approximate and probabilistic adders. IEEE Trans. Computers, 62(9):1760-1771, 2013.

Simulation Results of Approximate Adders

- 16-bit adders are simulated for all approximate designs.
- Each adder's name is followed by the value of its parameter *k*.
  - *k is the size of the sub-adder for ACA, ETAII, ESA, CSA, CSPA, CCA and GCSA.*
  - *k is the size of the less significant adder for LOA.*
- **100,000,000** random input combinations are simulated by MATLAB.



The MRED and NMED of approximate adders, sorted by MRED.

- The NMED and MRED show the same trend.
- ETAII, SCSA and ACAA have the same error characteristics (ER, NMED and MRED) due to the same carry propagation chain for each sum bit.

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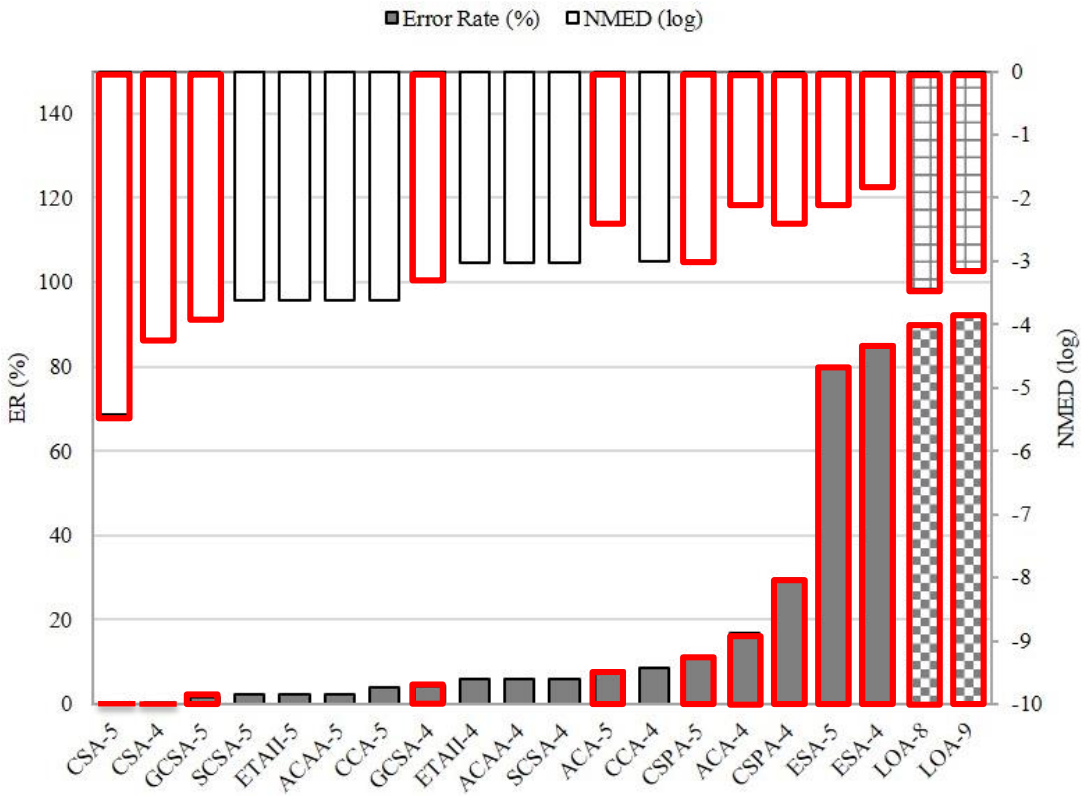
Error Characteristics of Approximate Adders [19]



The MRED and ER of approximate adders, sorted by ER.

- **LOA** has a rather **small MRED** but very **large ER**.
- **CSA-5** and **CSA-4** is the **most accurate**.
- **GCSA-5** and **GCSA-4** are the **second most accurate**.
- The information used to predict each carry in ESA, CSPA and ACA is rather limited, so the **MRED** and **ER** of **ESA** are the largest, followed by CSPA and ACA, when the same value of k is considered.
- **CCA, ETAII, SCSA** and **ACAA** shows moderate **MRED** and **ER**.

H. Jiang, J. Han and F. Lombardi, A Comparative Review and Evaluation of Approximate Adders, in GLSVLSI'15, Pittsburgh, PA, USA, 2015.

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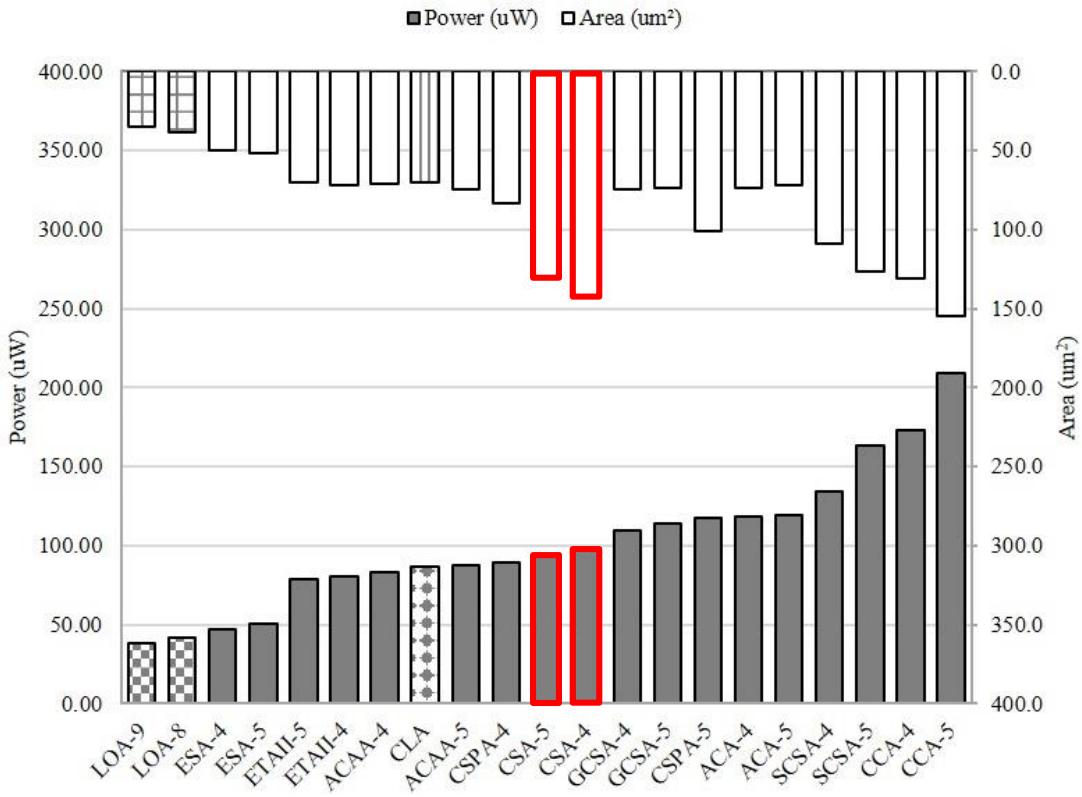
Circuit Characteristics of Approximate Adders

- All adders and sub-adders in the approximate designs are implemented as CLA.
- Synthesized by Synopsys Design Compiler based on an STM **28-nm** process with a supply voltage of **1.0V** at a temperature of **25 ºC**.



The power and area of approximate adders, sorted by power.

- A circuit with larger area is likely to consume more power except for **CSA** with low power dissipation but large area.
- This is due to its short critical path and enhanced carry select scheme and thus, complex wiring.

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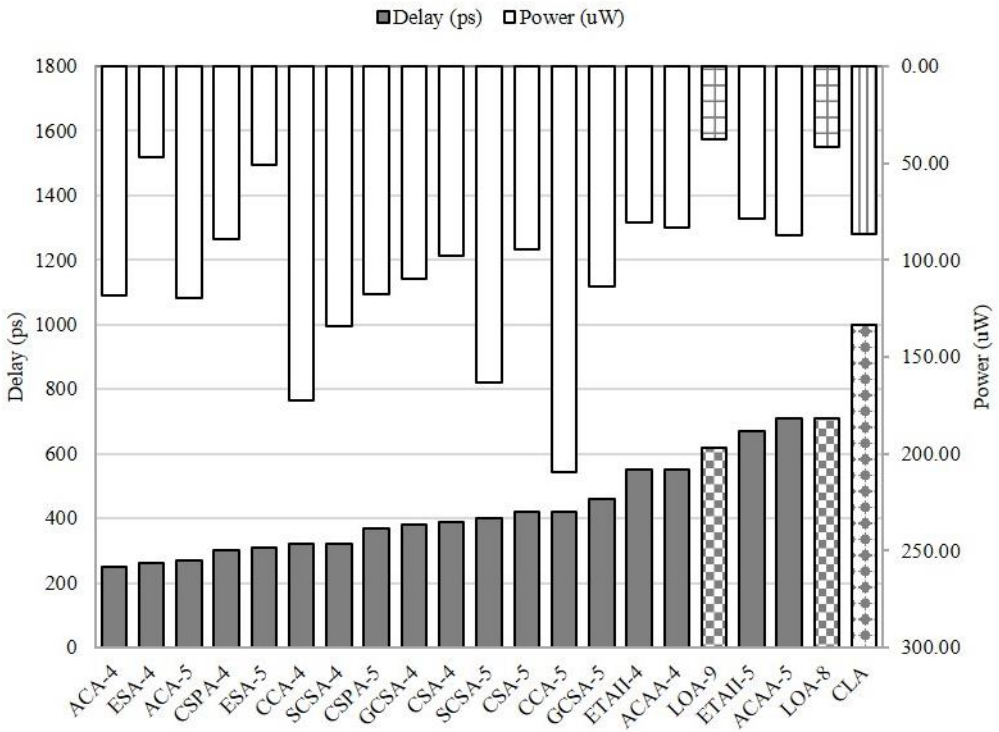
Circuit Characteristics of Approximate Adders



The power and delay of approximate adders, sorted by delay.

- Among **ETAII**, **SCSA** and **ACAA** (with the same accuracy), **SCSA** albeit being the **fastest**, incurs the **largest power** dissipation and **area**, and **ACAA** is the **slowest** because of its long critical path (2k). **ETAII** has a **shorter delay** than ACAA and consumes **less power** and requires a **smaller area** than SCSA.
- The **accurate CLA** has the **longest delay**, but **not the highest power dissipation**.
- **LOA** is very **slow**, but it is the **most power and area efficient.**

- Except for LOA and for the same k, **ACA** is the **fastest** and **power-wasting**, **ESA** is pretty **fast** and **power and area efficient**, **ACAA** is the **slowest**, and **CCA** is the **most power and area consuming** scheme.
- Both **CSPA** and **GCSA** have **moderate power dissipations**, but CSPA is faster and GCSA is more area efficient.

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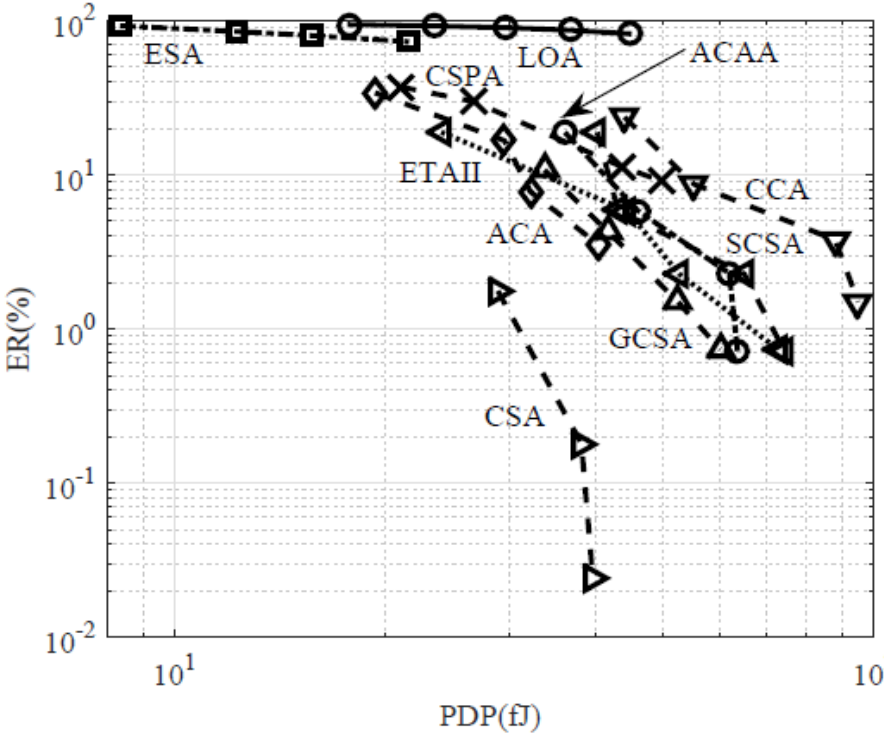
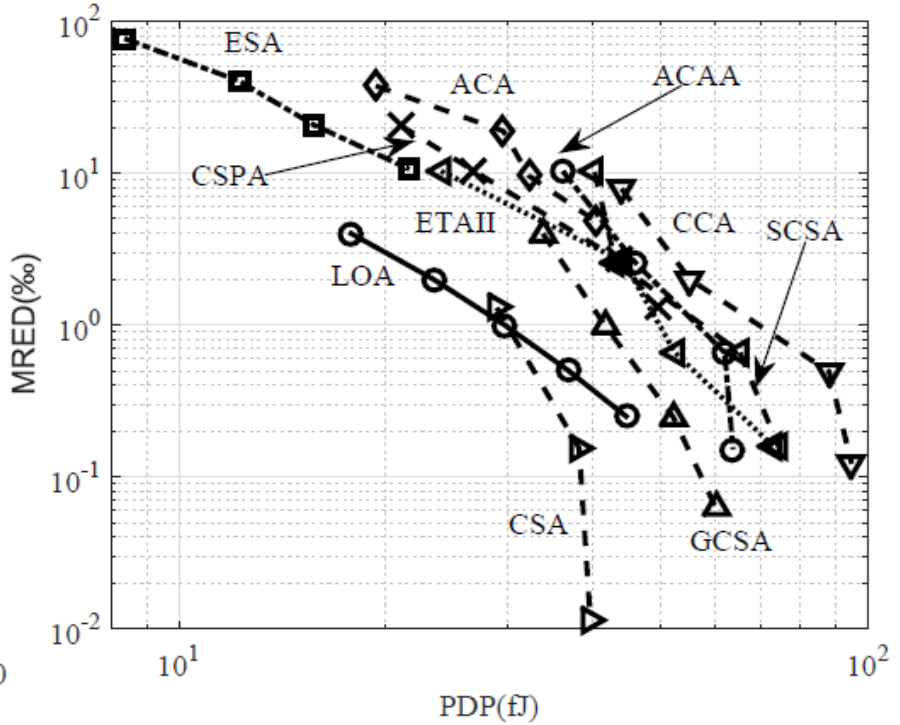
Considering Both Accuracy and Hardware



The ER and PDP of approximate adders.



The MRED and PDP of approximate adders.

- For the adders with the same accuracy, **ETAII, SCS**A and **ACAA**, **ETAII** has the **lowest PDP** (except for ETAII-6), while **SCSA** has the **highest**.
- **CSA** shows the **best performance** with very small PDP, ER and MRED.
- **ESA** has a rather **small PDP** but a considerably **large ER and MRED**.
- **ACA** has very **small PDP** and slightly lower ER and MRED than ESA.
- **CCA** has the **largest PDP** and **moderate ER** and **MRED**.
- **LOA** shows **small PDPs,** and its **MREDs** are **moderate** but with the **highest ER.**

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Conclusion on Approximate Adders

- In general, approximate speculative adders show moderate accuracy and relatively small PDPs.
- The approximate adders using approximate full adder in the LSBs are slow, but they are power efficient with high ERs (because of the approximate LSBs) and moderate NMED and MRED values because of the accurate MSBs).
- The error and circuit characteristics of the segmented and carry select adders vary with the predictions of carry signals.

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- Motivation and Introduction
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  - Circuit Characteristics
- **Review and Classification of Approximate Multipliers**
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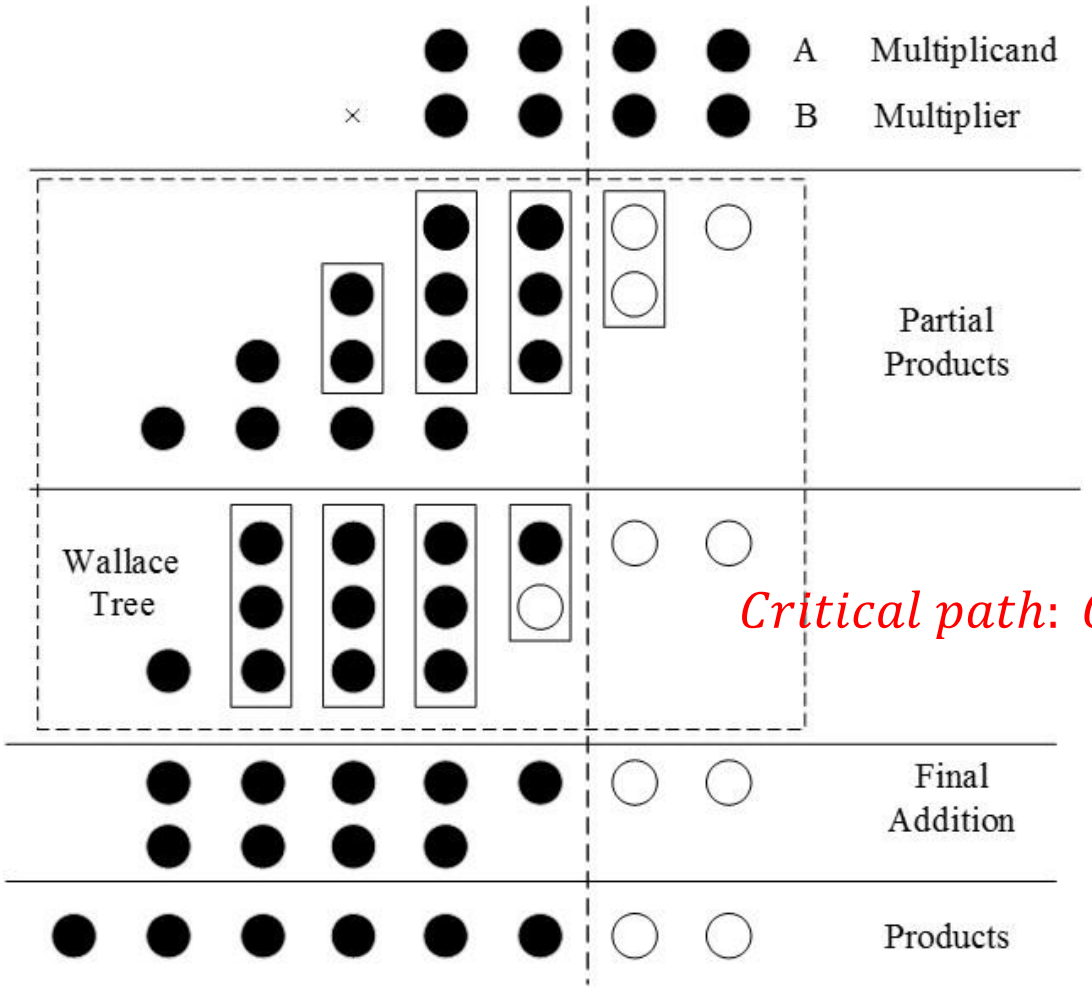
  - Error Characteristics
  - Circuit Characteristics
- **Conclusion**

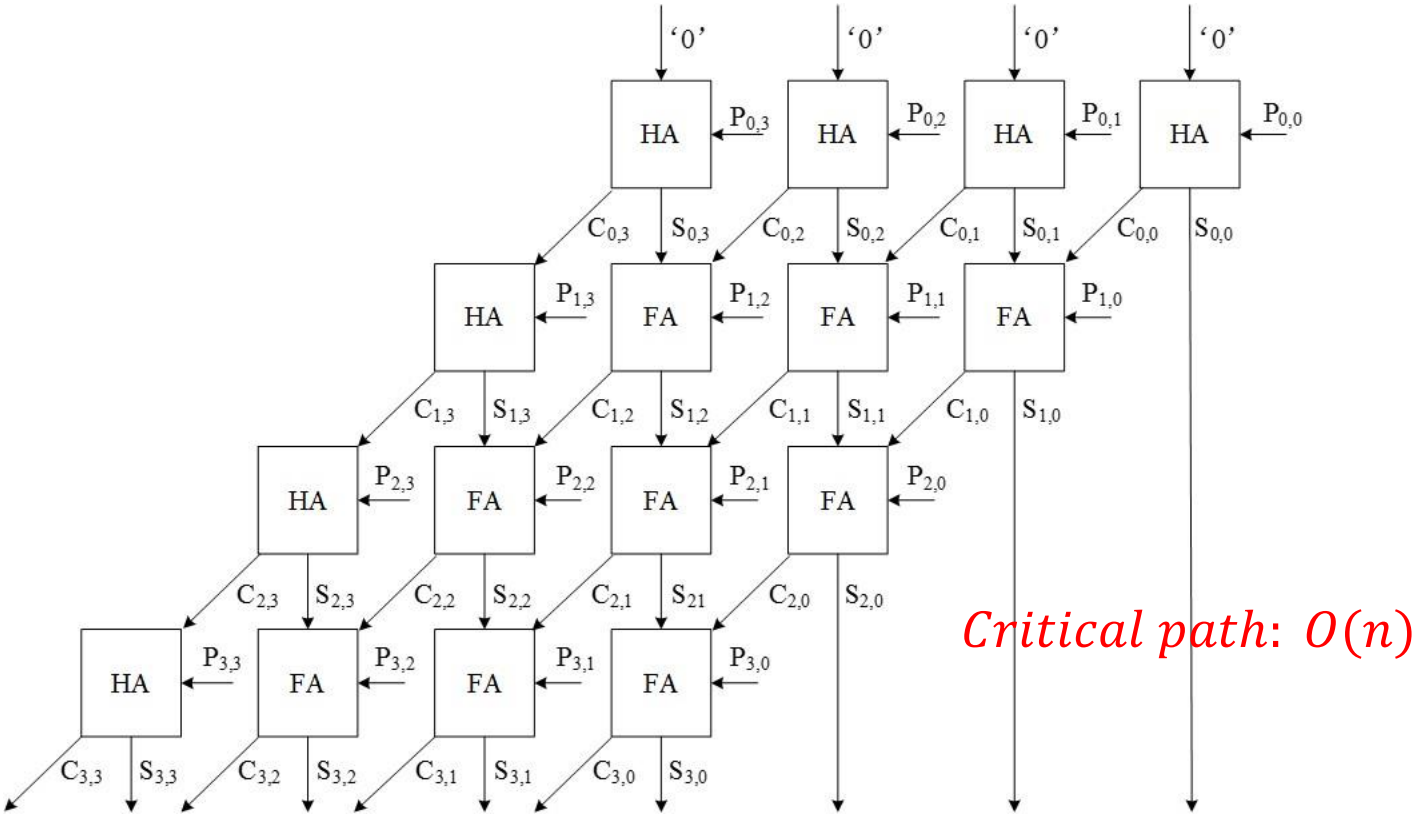
Multiplier: Wallace tree



$Critical\ path\colon\ O(\log(n))$

The basic arithmetic operation of a 4 x 4 bit unsigned multiplier

Multiplier: Carry-Save Adder Array



$Critical\ path\colon O(n)$

The partial product accumulation structure for a 4 x 4 bit unsigned multiplier using a carry-save adder array

Approximate Multipliers: A Classification

We classify the approximate multipliers into four categories:

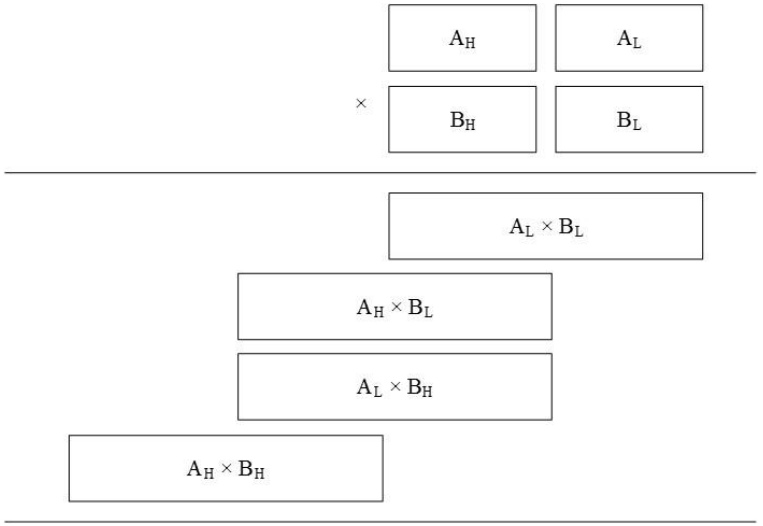
- **Approximation in Generating Partial Products**
  - Using simpler structure to generate partial products.
- **Approximation in the Partial Product Tree**
  - Omitting some partial products.
  - Dividing partial products into several sections and applying approximation in the less significant sections.
- **Using Approximate Counters or Compressors in the Partial Product Tree**
  - Approximating adders, counters or compressors
- **Approximate Booth Multipliers**

Approximation in Generating Partial Products

The Underdesigned Multiplier (UDM):

K-Map for the 2 x 2 bit underdesigned multiplier block

A_1A_0 \ B_1B_0	00	01	11	10
00	000	000	000	000
01	000	001	011	010
11	000	011	**1001**	110
10	000	010	110	100

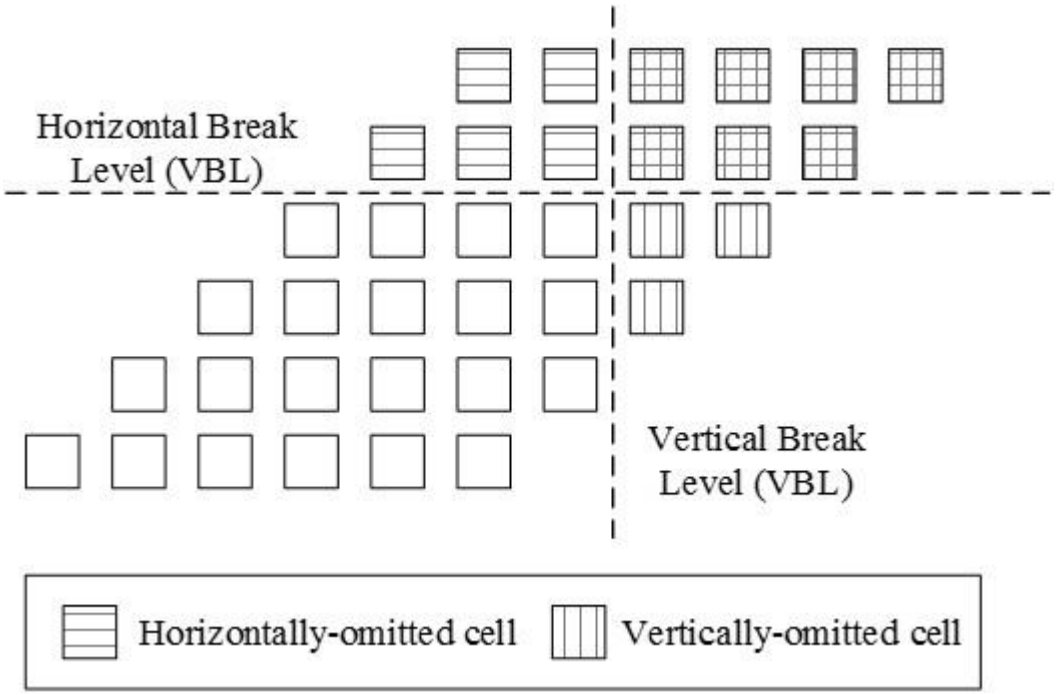


A 4 x 4 bit multiplier built on 2 x 2 bit block.

P. Kulkarni, P. Gupta, and M. Ercegovac, "Trading accuracy for power with an underdesigned multiplier architecture," in Proceedings of the 24th IEEE International Conference on VLSI Design, 2011, pp. 346–351.

Approximation in the Partial Product Tree (1)

The Broken-Array Multiplier (BAM):

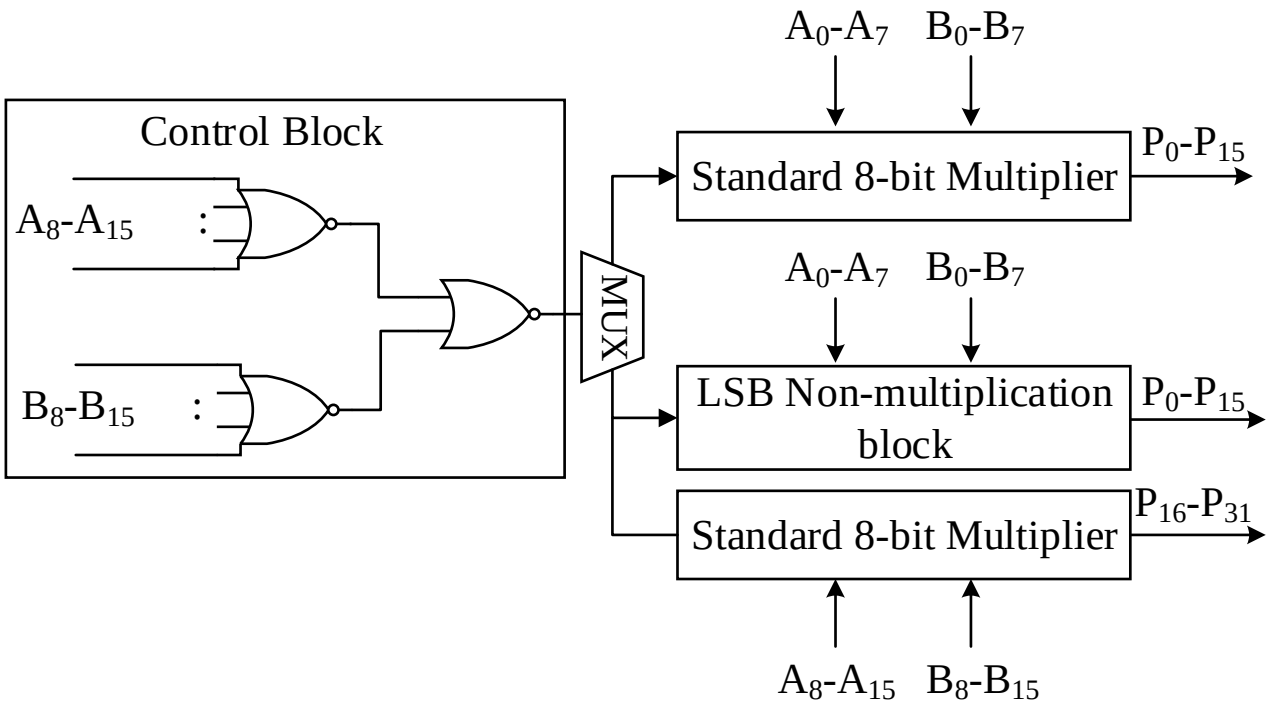


Structure of the Broken-Array Multiplier.

H. R. Mahdiani, A. Ahmadi, S. M. Fakhraie, and C. Lucas, "Bio-Inspired Imprecise Computational Blocks for Efficient VLSI Implementation of Soft-Computing Applications," IEEE Transactions on Circuits and Systems, vol. 57, no. 4, pp. 850–862, Apr. 2010.

Approximation in the Partial Product Tree (2)

The Error-Tolerant Multiplier (ETM):

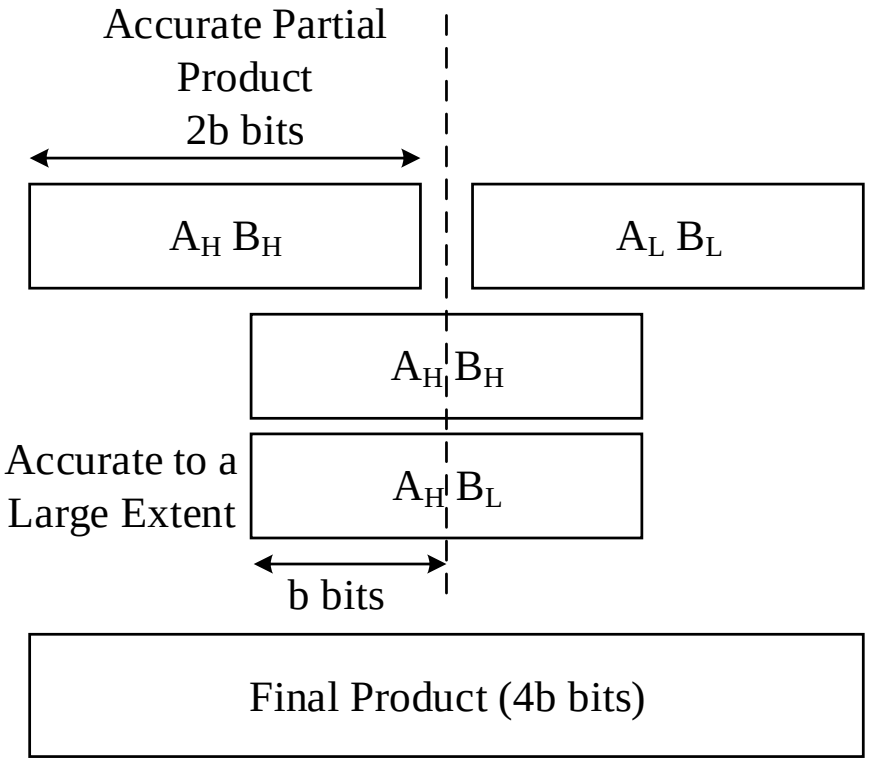


Architecture of a 16 x 16 bit Error-Tolerant Multiplier.

K. Y. Kyaw, W. L. Goh, and K. S. Yeo, "Low-power high-speed multiplier for error-tolerant application," in Proceedings of the 2010 IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC), 2010, pp. 1–4.

Approximation in the Partial Product Tree (3)

Approximate Wallace Tree Multiplier (AWTM):



Architecture of an Approximate Wallace Tree Multiplier.

K. Bhardwaj, P. S. Mane, and J. Henkel, "Power- and area-efficient Approximate Wallace Tree Multiplier for error-resilient systems," in Proceedings of the 15th International Symposium on Quality Electronic Design. IEEE, Mar. 2014, pp. 263–269.

Approximate Counters or Compressors (1)

Inaccurate Counter based Multiplier (ICM):

K-Map for the inaccurate 4:2 counter for 4 x 4 bit Wallace multiplier

X_3X_4 \ X_1X_2	00	01	11	10
00	00	01	10	01
01	01	10	11	10
11	10	11	**10**	11
10	01	10	11	10

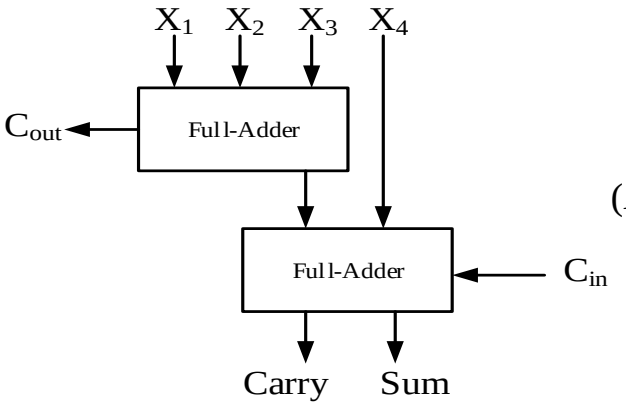
CS

Larger Multipliers are implemented by the inaccurate 4 x 4 bit multiplier.

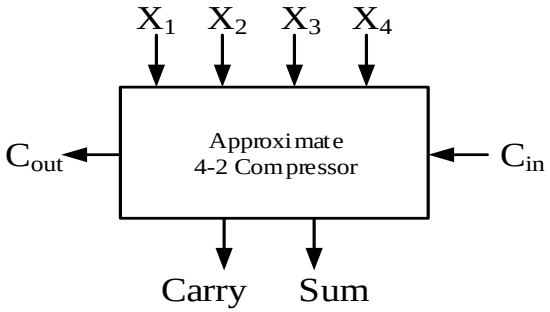
C.-H. Lin and I.-C. Lin, "High accuracy approximate multiplier with error correction," in Proceedings of the 31st IEEE International Conference on Computer Design (ICCD 2013). pp. 33–38. Oct. 2013.

Approximate Counters or Compressors (2)

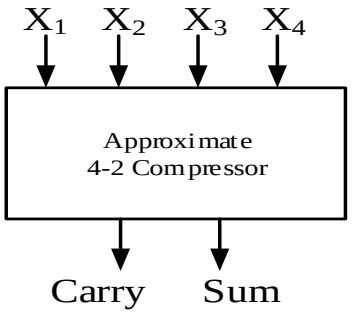
Approximate Compressor based Multiplier (ACM):



Accurate 4-2 compressor.



Approximate 4-2 compressor design 1 (AC1): altering 12 out of 32 K-Map entries.



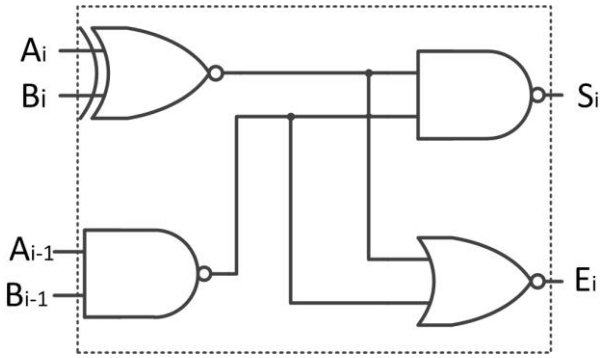
Approximate 4-2 compressor design 2 (AC2): altering 4 out of 16 K-Map entries.

ACM-3: AC1 in LSBs and accurate compressors in MSBs in a Dadda multiplier.
ACM-4: AC2 in LSBs and accurate compressors in MSBs in a Dadda multiplier.

A. Momeni, J. Han, P. Montuschi, and F. Lombardi, "Design and Analysis of Approximate Compressors for Multiplication," IEEE Transactions on Computers, vol. 64, no. 4, pp. 984–994, 2015.

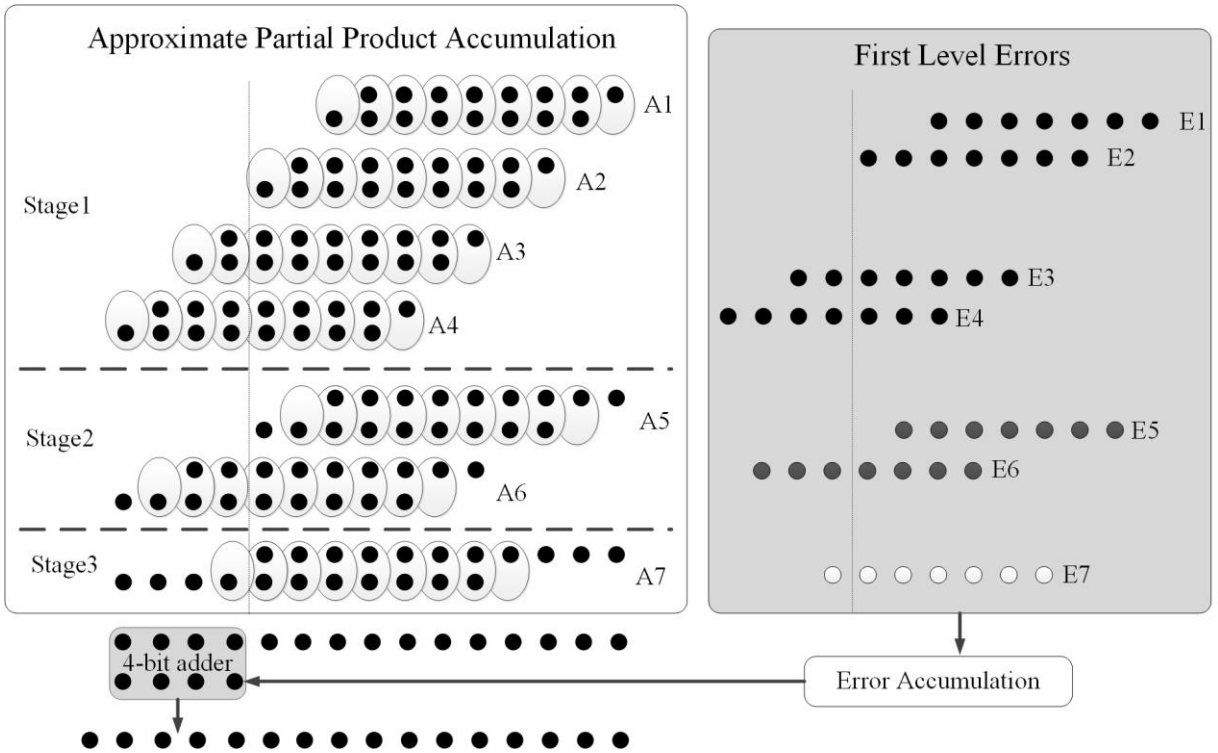
Approximate Counters or Compressors (3)

Approximate Multiplier (AM) with Configurable Partial Error Recovery and Truncated AM (TAM):



The approximate adder cell.

- Two error accumulation trees are designed for AM1 and AM2.
- TAM1 and TAM2 are obtained by truncating some LSBs.

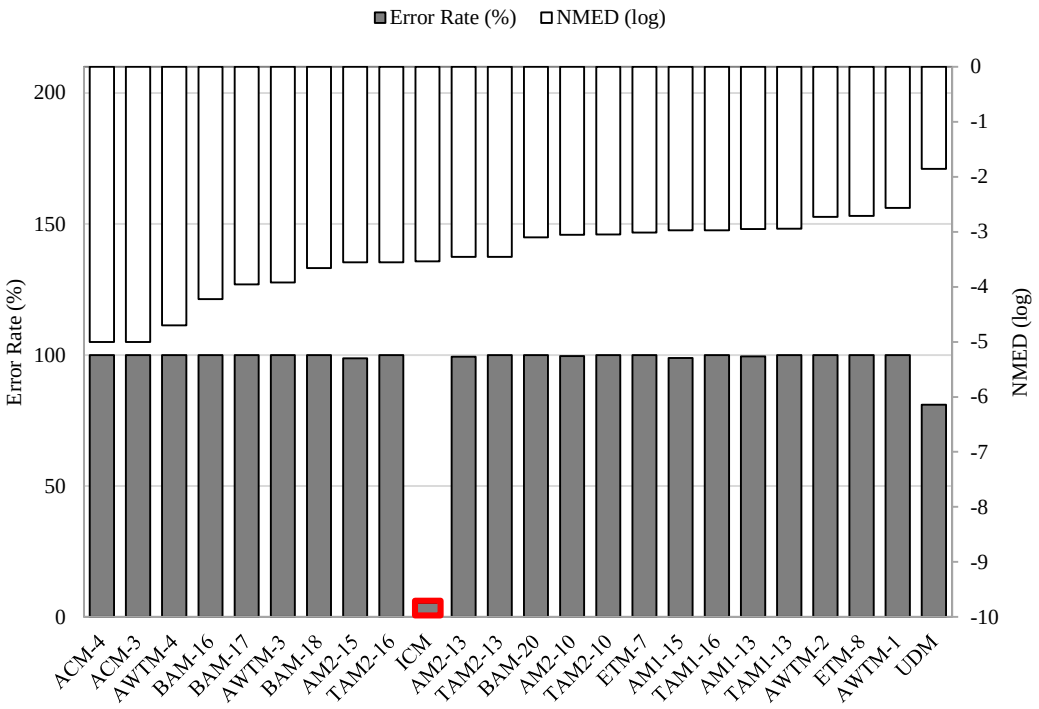


The approximate multiplier with 4-bit error recovery.

C. Liu, J. Han, and F. Lombardi, "A low-power, high-performance approximate multiplier with configurable partial error recovery," DATE, 2014.

Simulation Results of Approximate Multipliers

- 16 x 16 bit multipliers are simulated for all approximate designs.
- Each multiplier's name is followed by the value of its parameter *k*.
  - *k is the number of MSBs used for error reduction in AM1, AM2, TAM1 and TAM2.*
  - *k is the number of LSBs in the inaccurate part for ETM.*
  - *k is the mode number in AWTM and ACM.*
  - *It is the vertical broken length for BAM.*
- **100,000,000** random input combinations are simulated by MATLAB.



The ER and NMED of approximate multipliers, sorted by NMED.

- **ICM** has a very low **ER** of **5.45%**, because it uses just one approximate compressor in a 4 × 4 bit sub-multiplier with an error rate of only 1/256.
- Most of the designs, especially those with truncation, have large ERs (nearly **100%**).

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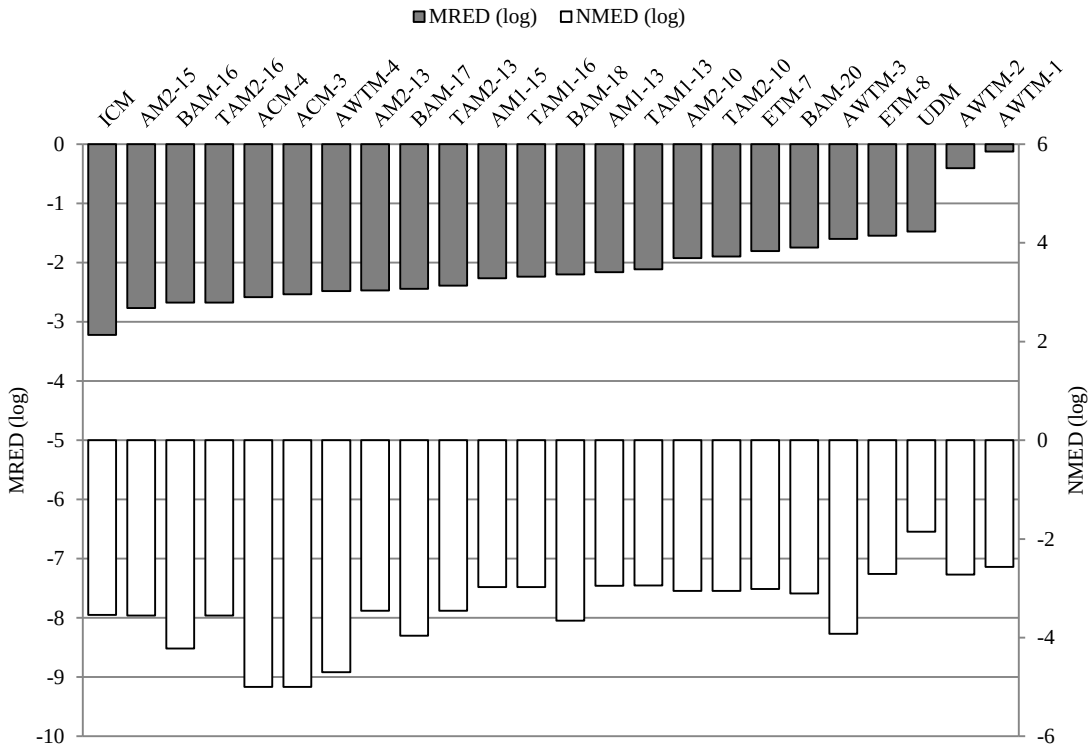
Error Characteristics of Approximate Multipliers



The MRED and NMED of approximate multipliers, sorted by MRED.

- **ICM**, **AM2-15** and **TAM2-16** have close NMED values, however **ICM** has the **smallest MRED** while the MRED of **TAM2-16** is the largest.
- Multipliers with truncation (**TAM2-16** and **BAM-18**) tend to have larger MREDs when NMEDs are similar.
- **ACM-4**, **ACM-3** and **AWTM-4** achieve very **low NMEDs** because only LSBs are approximated in them.
- **ETM** and **BAM** have relatively **large MREDs** due to truncation.

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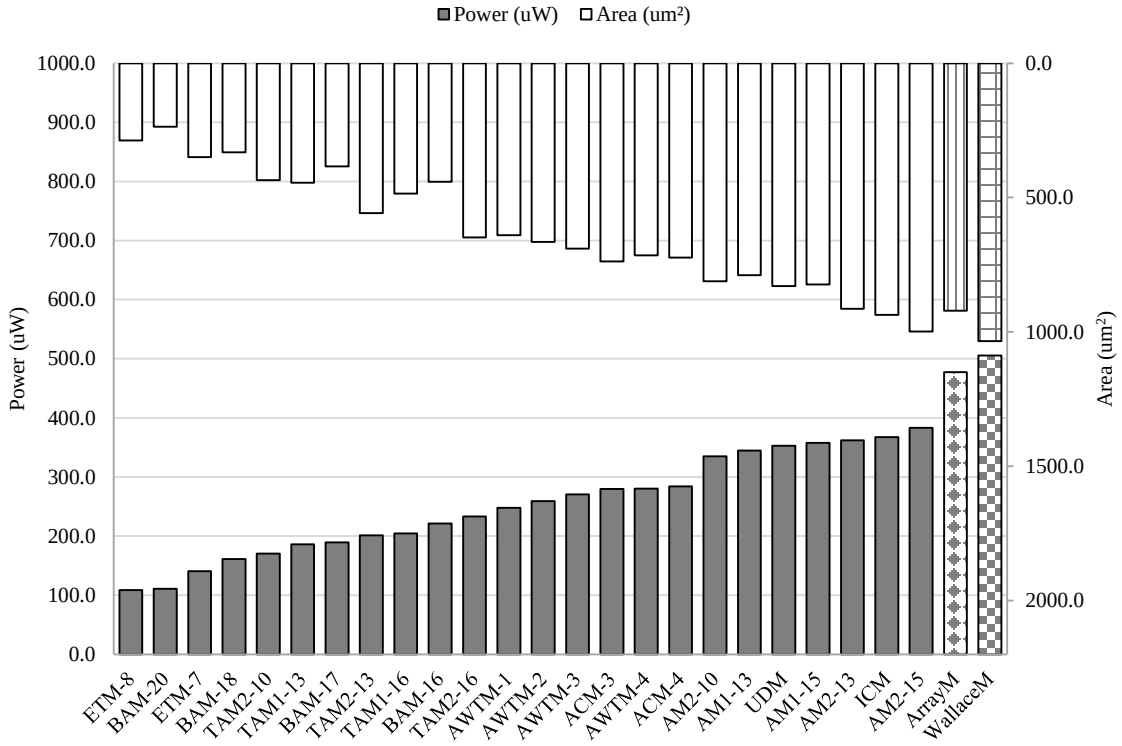
Circuit Characteristics of Approximate Multipliers (1)

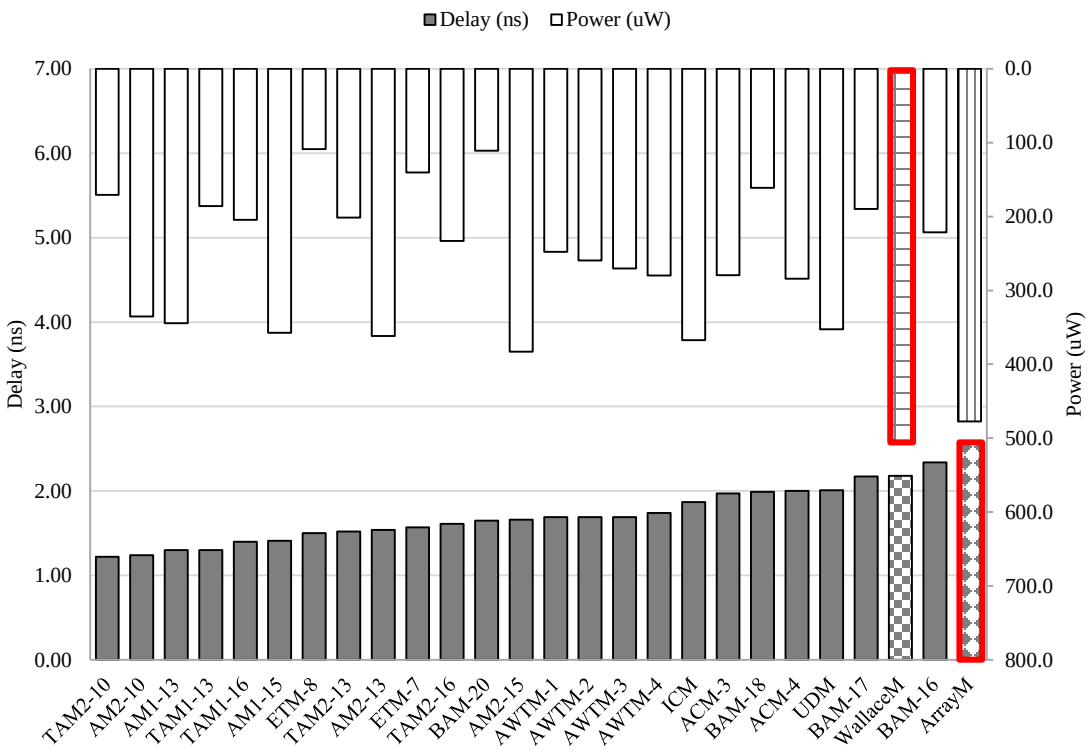
- 16 x 16 bit multipliers are implemented in VHDL for all approximate designs.
- Synthesized by Synopsys Design Compiler based on an STM **28-nm** process with a supply voltage of **1.0V** at a temperature of **25 ºC**.



The power and area of approximate multipliers, sorted by power.

- A multiplier with larger area is likely to consume more power.

Circuit Characteristics of Approximate Multipliers (2)

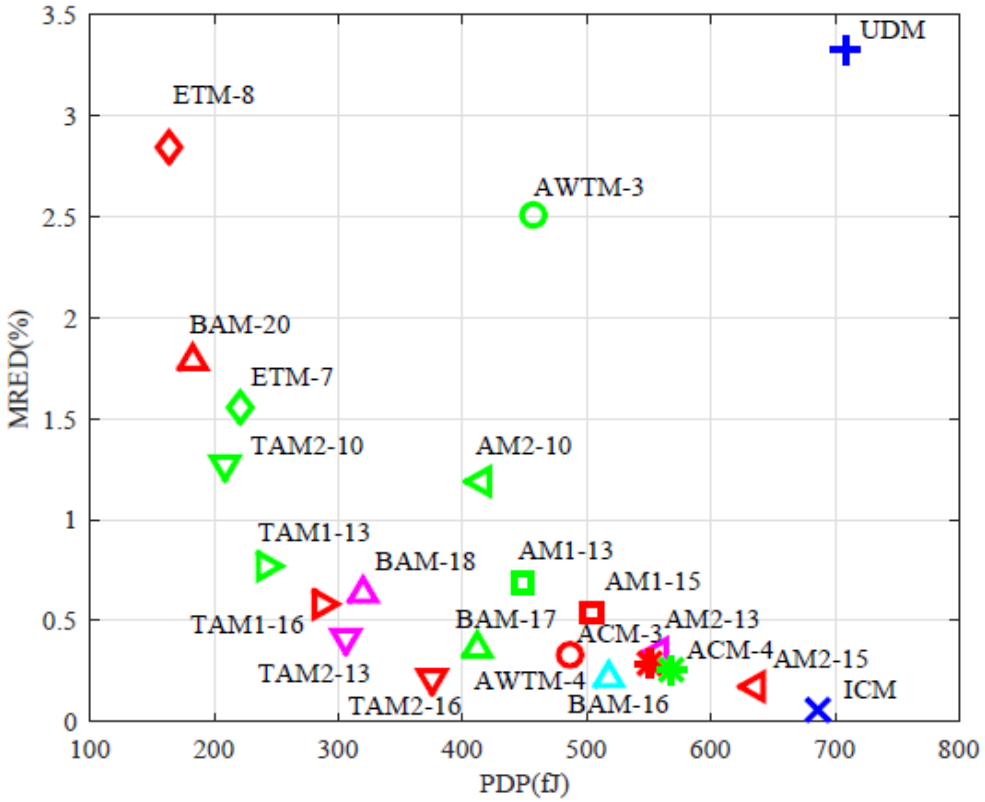


The delay and power of approximate multipliers, sorted by delay.

- **ETM, TAM1/TAM2** and **BAM are among the most power efficient** designs**.**
- **Truncation** is a useful approach to **reduce power and area.**

- **ArrayM** is the **slowest.**
- **WallaceM** is the **most power consuming.**
- **AM1,TAM1, AM2** and **TAM2** have **smaller delays** even with a 16-bit error reduction.
- **BAM** is significantly **slow** due to its array structure.
- **AWTM, UDM, ICM** and **ACM** have **larger delays** than the other multipliers.
- **BAM** consumes very **low power**, the power consumption of **AWTM** and **ACM** are **in the middle range**, while **UDM** and **ICM** incur relatively **high power** consumption.

Considering Both Accuracy and Hardware



The MRED and PDP of approximate multipliers.

- **TAM1-13, TAM-16, TAM2-13** and **BAM-18** have both **small PDPs** and **MREDs**
- **ICM** and **ACM** incur an very **low error**, but their **PDPs** are very **high**.
- **BAM-22** has the **smallest PDP** but **largest MRED**.
- **ETM-8** has the **smallest PDP** but significantly **large MRED**.
- **UDM** shows **poor** performance in both **PDP** and **MRED.**
- **ETM** has a **small PDP** and a relatively **large MRED**.
- Most **BAM** configurations have **small PDPs**, their d**elays** are generally **large**.

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Conclusion on Approximate Multipliers

- Truncation on part of the partial products is an effective methodology to save hardware. However, it incurs a large ER but moderate NMED and MRED.
- Approximate multipliers implemented by smaller approximate sub-multipliers may have very low ERs (e.g., UDM and AWTM-3), but their NMEDs and MREDs are usually large because of the large errors that may occur in the more significant part of the multiplier. Moreover, they usually have rather high PDPs.

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Thanks for your attention.
Questions?